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| TRANSMITTAL OF APPEAL BRIEF | Docket No. SON-1661 |
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In re Application of: Yoshihiko Imamura

| Application No. | Filing Date | Examiner | Group Art Unit |
|---|---|---|---|
| 09/420,798 | October 19, 1999 | G. Opie | 3308 |

Invention: PARALLEL PROCESSOR, PARALLEL PROCESSING METHOD, AND STORING MEDIUM

**TO THE COMMISSIONER OF PATENTS:**

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed: November 21, 2003 .



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Dated: January 21, 2004

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#14/Appeal Br. of McBeth-Brown 2/5/04



Docket No.: SON-1661 (PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of:
Yoshihiko IMAMURA

Confirmation No.: 3308

Application No.: 09/420,798

Art Unit: 2126

Filed: October 19, 1999

Examiner: G. Opie

For: PARALLEL PROCESSOR, PARALLEL PROCESSING METHOD, AND STORING MEDIUM



**APPELLANT'S BRIEF**

**MS Appeal Brief - Patents**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is an Appeal Brief filed under 37 C.F.R. § 1.192 appealing the Final Rejection of the Primary Examiner dated September 22, 2003 (Paper No. 9). A Notice of Appeal was timely filed on November 21, 2003. The fees required under § 1.17(f), and any required petition for extension of time for filing this brief and fees therefore, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF. This brief is transmitted in triplicate.

This brief contains items under the following headings as required by 37 C.F.R. § 1.192 and M.P.E.P. § 1206:

I. Real Party in Interest
II Related Appeals and Interferences
III. Status of Claims
IV. Status of Amendments
V. Summary of Invention
VI. Issues
VII. Grouping of Claims

VIII. Arguments
IX. Claims Involved in the Appeal

Appendix A: Claims

## I. REAL PARTY IN INTEREST

Sony Corporation of Tokyo, Japan ("Sony") is the real party in interest of the present application. An assignment of all rights in the present application to Sony was executed by the inventor and recorded by the U.S. Patent and Trademark Office on January 10, 2000 at **Reel 10480, Frame 330**.

## II. RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences related to the present application of which the Appellant is aware that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending matter.

## III. STATUS OF CLAIMS

### A. Total Number of Claims in Application

There are twenty-two (22) claims currently pending in the present application, consisting of claims 23-44, each of which stands finally rejected. No claims are currently allowed. Accordingly, the Appellants hereby appeal the final rejection of claims 23-44, each of which is presented in Appendix A.

### B. Current Status of Claims

1. Claims cancelled: 1-22
2. Claims withdrawn from consideration but not cancelled: None
3. Claims pending: 23-44
4. Claims allowed: None
5. Claims rejected: 23-44

### C. Claims on Appeal

The claims on appeal are claims 23-44.

## IV. STATUS OF AMENDMENTS

The application as originally filed contained claims 1-22. A Preliminary Amendment was filed on October 19, 1999 in order to correct various grammatical informalities in the specification and in claims 1, 3-5, 10, 12-16, 18, and 20-22. In response to the First Office Action on the merits dated March 12, 2003 (Paper No. 6), Appellant cancelled claims 1-22 and added new claims 23-44. In response to the Second Office Action on the merits dated September 22, 2003 (Paper No. 9), Appellant filed an Amendment on October 17, 2003 canceling claims 28 and 40 and amending claims 23, 24, 26, 36, 38, 39 and 43. The examiner, however, by way of the Advisory Action mailed November

6, 2003 (Paper No. 12), declined to enter Appellant's Amendment filed October 17, 2003, instead stating that the proposed amendments would only be entered upon the timely submission of a Notice of Appeal and Appeal Brief. Claims 23-44 thus stand finally rejected. The claims as amended and as originally submitted in Appellant's Amendment of October 17, 2003 have been re-presented in Appendix A. Accordingly, Appellant respectfully requests the entry of the claims as set forth in Appendix A.

## V. SUMMARY OF INVENTION

The present invention is directed to a parallel processor, parallel processing method and storing medium for storing the routine of the method in a computer readable format.

An object of the present invention is to provide a parallel processor and a parallel processing method enabling various forms of synchronization among programs executed in parallel and a storing medium for storing the routine of the method in a computer-readable format. (See page 10, lines 8-13).

A second object of the present invention is to provide a parallel processor which can shorten a waiting time of a processor element caused by the transfer of a user program between a local memory of the processor element and a common memory. (See page 10, lines 13-17).

As described on pages 10-16 of the specification, various embodiments of the present invention are provided in order to accomplish the above-recited objectives. According to a first aspect of the invention, a parallel processor is provided comprising a plurality of processing means which perform mutually parallel processing on the basis of instructions written in programs and are capable of communicating with each other via a common bus. One of the processing means then either suspends processing based on a program and enters a waiting

state when executing a wait instruction, or releases the waiting state and restarts the processing based on the program based on execution of a wait release instruction by another processing means. The other processing means then executes a next instruction without suspending processing after it executes the wait release instruction.

Synchronization is established between one processing means and another processing means at the instruction level while executing both programs by using a wait instruction and a wait release instruction in the programs. Namely, it is possible to synchronize programs without having to wait for the completion of an execution of one program. Accordingly, the execution of a wait instruction in one processing means prior to the execution of a wait release instruction in another processing means can be prevented. (See page 11, lines 23-25). Various other embodiments and improvements to the bases of this invention have been set forth in greater detail on pages 10-16 of the specification.

## VI. ISSUES

The issues presented for consideration in this appeal are as follows:

(1) Whether the Examiner erred in rejecting claims 23 and 28-29 under 35 U.S.C. § 102(a) as being anticipated by the Admitted Prior Art ("APA")?

(2) Whether the Examiner erred in rejecting claims 23-44 under 35 U.S.C. § 103(a) as being unpatentable over the Admitted Prior Art ("APA") detailed on pages 1-7 of the Background Section of the Appellant's Application in view of U.S. Patent No. 5,634,071 to Dewa et al. ("Dewa")?

## VII. GROUPING OF CLAIMS

For purposes of the issues presented by this appeal:

Claims 23, 25, 27, 29, 30-35 stand or fall together.

Claims 36, 37, 41 and 42 stand or fall together.

Claim 24 stands or falls separately.

Claim 26 stands or falls separately.

Claim 38 stands or falls separately.

Claim 39 stands or falls separately.

Claim 43 stands or falls separately.

Claim 44 stands or falls separately.

The arguments set forth in the following section provide reasons why these groups are considered separately patentable, as required by 37 C.F.R. 1.192 (c)(7).

## VIII. ARGUMENTS

### A. Claims 23 and 28-29 Are Not Anticipated by the Admitted Prior Art

Claims 23 and 28-29 were rejected under 35 U.S.C. § 102(a) as allegedly being anticipated by the Admitted Prior Art disclosed on pages 1-7 of the Background Section of the Specification of the present invention.

As set forth in Appendix A, independent claim 23 has been amended so as to wholly incorporate the limitations of prior claim 28. Claim 28 has been subsequently cancelled.

Claim 23, as currently amended in Appendix A, recites a parallel processor wherein, *inter alia*, a first processor

element executes a program end instruction, the program end instruction serving to resume the processing of a second user program.

The APA, in contrast, fails to disclose, teach or suggest a first processor element executing a program end instruction serving to resume the processing of a second user program. In particular, Figure 8 represents a configuration of the APA arguably depicting processor elements 111 through 114. On pages 2 and 3 of the Final Office Action dated September 22, 2003, the examiner argues that Figure 8 teaches of a first processing element 111 and a second processor element 114. Even if this were the case, Figure 8 of the APA still fails to disclose, teach or suggest the first processor element 111 as executing a program end instruction and as resuming processing of the second user program 114. No findings to the contrary have been made by the examiner.

Accordingly, since each and every limitation is not found within the applied art, the rejection of claim 23 fails to establish a *prima facie* rejection, and withdrawal thereof is respectfully requested. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Accord. M.P.E.P. § 2131.

Moreover, aside from the novel limitations recited therein, dependent claim 29, being dependent upon independent claim 23, also represents allowable subject matter for at least the reasons set forth above. Withdrawal of the rejection of this claims is therefore respectfully requested.

**B. Claims 23-44 Are Not Obvious in View of the Admitted Prior Art and Further in View of Dewa**

Claims 23-44 stand finally rejected under 35 U.S.C. § 103(a) as allegedly being obvious in view of the Admitted Prior Art ("APA") detailed on pages 1-7 of the Background Section of the Appellant's Application and further in view of U.S. Patent No. 5,634,071 to Dewa. The test for obviousness is what the combined teachings of the prior art would have suggested to one of ordinary skill in the art. *See, e.g., In re Keller*, 642 F. 2d 413, 425, 208 USPQ 871, 881 (CCPA 1981). In establishing a *prima facie* case of obviousness, it is incumbent upon the Examiner to provide a reason why one of ordinary skill in the art would have been led to modify a prior art reference or to combine reference teachings to arrive at the claimed invention. *See Ex parte Clapp*, 227 USPQ 972, 973 (Bd.Pat.App. & Interf. 1985). To this end, the requisite motivation must stem from some teaching, suggestion or inference in the prior art as a whole or from the knowledge generally available to one of ordinary skill in the art, and not from the Appellant's disclosure. To reach this analysis, proper findings are required.

It is fundamental to this appeal that the findings of fact upon which the Examiner relied to consider the claims are not accurate or supported by substantial evidence. Therefore, the Examiner has failed to make a *prima facie* finding of obviousness sufficient to withstand this scrutiny. Therefore, for at least the reasons set forth in greater detail below, the rejection of claims 23-44 should be reversed.

1. Claims 23, 25, 27, 29, 30-35 are Not Obvious

As is set forth in Appendix A, independent claim 23 has been amended so as to wholly incorporate the limitations of prior claim 28. Claim 28 has been subsequently cancelled.

Claim 23, as currently amended in Appendix A, recites a parallel processor wherein, *inter alia*, a first processor element executes a program end instruction, the program end instruction serving to resume the processing of a second user program.

The APA, in contrast, fails to disclose, teach or suggest a first processor element executing a program end instruction serving to resume the processing of a second user program. In particular, Figure 8 represents a configuration of the APA arguably depicting processor elements 111 through 114. On pages 2 and 3 of the Final Office Action dated September 22, 2003, the examiner argues that Figure 8 teaches that these elements represent a first processing element 111 and a second processor element 114. Even if this were the case, Figure 8 of the APA still fails to disclose, teach or suggest the first processor element 111 as executing a program end instruction and as resuming processing of the second user program 114, as is recited in claim 23. No findings to the contrary have been made by the examiner. The application of the Dewa reference additionally fails to remedy this deficiency.

Accordingly, Appellants assert that the rejection of claim 23 fails to establish a *prima facie* case of obviousness because there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings.[1]

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. [2] To do so would be an impermissible use of hindsight reconstruction

[1] *In re Linter*, 458 F.2d 1013, 173 USPQ 560, 562 (CCPA 1972).
[2] *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

from Appellants' disclosure.[3] It would appear that any suggestion or motivation of such a replacement or substitution as suggested by the Examiner flows, not from the prior art going forward toward the invention claimed, but in a hindsight manner based on the teachings of the specification. For the claimed combination, there are no motivating teachings found to support factually the proposed substitution in light of the foregoing arguments. Withdrawal of this rejection is therefore respectfully requested.

Moreover, aside from the novel limitations recited therein, dependent claims 25, 27, 29 and 30-35, being dependent either directly or indirectly upon independent claim 23, also represent allowable subject matter for at least the reasons set forth above. Withdrawal of the rejection of these claims is therefore respectfully requested.

2. Independent Claim 24 is Not Obvious

Independent claim 24, as currently amended in Appendix A, recites a parallel processor wherein, *inter alia*, the second processor element executes a synchronization wait instruction which suspends processing of the second user program, and the wait instruction suspends processing of the first user program while resuming the processing of the second user program.

On page 3 of the Office Action dated September 21, 2003, the examiner contends that the Appellant's related art teaches the second processor element 114 as executing an "end" as a wait release instruction such that the "end" commands the first processor element 111 to resume the processing of the first user program. However, while Figure 8 of the Appellant's related art arguably teaches of an "end" instruction processed by the

[3] *In re Dembiczak*, 50 USPQ2d 1614 (Fed. Cir. 1999).

alleged second processor element 114, Figure 8 of the Appellant's related art fails to disclose, teach or suggest the second processor element 114 as also executing a synchronization wait instruction that suspends processing of the second user program 114, as is recited in independent claim 24 of the present invention. This feature was not addressed within the Final Office Action of September 22, 2003. In this regard, the Final Office Action merely contends that the first processing element 111 of Figure 8 enters into a synchronized waiting state.

In addition, Figure 8 of the Appellant's related art fails to disclose, teach or suggest the wait instruction suspending processing of the first user program while resuming the processing of the second user program. As with the previous element, this feature has not been addressed within the Final Office Action. The application of the Dewa reference additionally fails to remedy this deficiency.

Accordingly, since the applied art fails to teach each and every limitation of claim 24, a *prima facie* rejection of the claims has not been established and withdrawal thereof is respectfully requested. [3]

3. Independent Claim 26 is Not Obvious

Independent claim 26, as set forth in Appendix A, recites a parallel processor wherein, *inter alia*, the second processor element executes a next instruction without suspending the processing of the second user program after executing the wait release instruction.

In contrast, Figure 8 of the Appellant's related art fails to disclose, teach or suggest the second processor element 114

[3] *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

executing a next instruction without suspending the processing of the second user program after executing the alleged wait release instruction ("end"). Instead, Figure 8 of the Appellant's related art depicts the termination of the second user program after executing the alleged wait release instruction ("end"). The application of the Dewa reference additionally fails to remedy this deficiency.

Accordingly, since the applied art fails to teach each and every limitation of claim 26, a *prima facie* rejection of the claims has not been established and withdrawal thereof is respectfully requested.

4. Claims 36, 37, 41 and 42 are Not Obvious

As is set forth in Appendix A, independent claim 36 has been amended so as to wholly incorporate the limitations of prior claim 40. Claim 40 has been subsequently cancelled.

Claim 36, as currently amended in Appendix A, recites a parallel processor wherein, *inter alia*, a first processor element executes a program end instruction, the program end instruction serving to resume the processing of a second user program.

The APA, in contrast, fails to disclose, teach or suggest a first processor element executing a program end instruction serving to resume the processing of a second user program. In particular, Figure 8 represents a configuration of the APA arguably depicting processor elements 111 through 114. On pages 2 and 3 of the Final Office Action dated September 22, 2003, the examiner argues that Figure 8 teaches of a first processing element 111 and a second processor element 114. Even if this were the case, Figure 8 of the APA still fails to disclose, teach or suggest the first processor element 111 as executing a program end instruction and as resuming processing of the second

user program 114. No findings to the contrary have been made by the examiner. The application of the Dewa reference additionally fails to remedy this deficiency.

Accordingly, since the applied art fails to teach each and every limitation of claim 36, a *prima facie* rejection of the claims has not been established and withdrawal thereof is respectfully requested.

Moreover, aside from the novel limitations recited therein, dependent claims 37, 41 and 42, being dependent either directly or indirectly upon independent claim 36, also represent allowable subject matter for at least the reasons set forth above. Withdrawal of the rejection of these claims is therefore respectfully requested.

5. Independent Claim 38 is Not Obvious

Independent claim 38, as currently amended in Appendix A, recites a parallel processor wherein, *inter alia*, the second processor element executes a synchronization wait instruction which suspends processing of the second user program, and the wait instruction suspends processing of the first user program while resuming the processing of the second user program.

On page 3 of the Office Action dated September 21, 2003, the examiner contends that the Appellant's related art teaches the second processor element 114 as executing an "end" as a wait release instruction such that the "end" commands the first processor element 111 to resume the processing of the first user program. However, while Figure 8 of the Appellant's related art arguably teaches of an "end" instruction processed by the alleged second processor element 114, Figure 8 of the Appellant's related art fails to disclose, teach or suggest the second processor element 114 as also executing a synchronization wait instruction that suspends processing of the second user

program 114. This feature was not addressed within the Final Office Action of September 22, 2003. In this regard, the Final Office Action contends that the first processing element 111 of Figure 8 enters into a synchronized waiting state.

In addition, Figure 8 of the Appellant's related art fails to disclose, teach or suggest the wait instruction suspending processing of the first user program while resuming the processing of the second user program. As with the previous element, this feature has not been addressed within the Final Office Action. The application of the Dewa reference additionally fails to remedy this deficiency.

Accordingly, since the applied art fails to teach each and every limitation of claim 38, a *prima facie* rejection of the claims has not been established and withdrawal thereof is respectfully requested.

6. Independent Claim 39 is Not Obvious

Independent claim 39, as set forth in Appendix A, recites a parallel processor wherein, *inter alia*, the second processor element executes a next instruction without suspending the processing of the second user program after executing the wait release instruction.

In contrast, Figure 8 of the Appellant's related art fails to disclose, teach or suggest the second processor element 114 executing a next instruction without suspending the processing of the second user program after executing the alleged wait release instruction ("end"). Instead, Figure 8 of the Appellant's related art depicts the termination of the second user program after executing the alleged wait release instruction ("end"). The application of the Dewa reference additionally fails to remedy this deficiency.

Accordingly, since the applied art fails to teach each and

every limitation of claim 39, a *prima facie* rejection of the claims has not been established and withdrawal thereof is respectfully requested.

7. Independent Claim 43 is Not Obvious

Independent claim 43, as presented in Appendix A, recites a storage medium for storing in a computer-readable format routines wherein, *inter alia*, the second processing enters a synchronization waiting state by executing the wait release instruction until the first processing enters the waiting state when the first processing is not in the waiting state.

In contrast, the teachings of Dewa and that of Appellant's related art, either individually or in combination, fail to teach, disclose or suggest second processing entering a synchronization waiting state by executing the wait release instruction until the first processing enters the waiting state when the first processing is not in the waiting state. While the examiner contends that having the second processor pause for synchronization when executing the release instruction would naturally have flowed from Dewa's parallel process coordination teachings, these unsupported assertions amount to nothing more than conclusions that are personal in nature. In this regard, the teachings, suggestions or incentives supporting the obviousness-type double patenting rejection must be clear and particular. Broad conclusory statements, standing alone, are insufficient as evidence. *In re Dembiczak*, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

As a rule, "assertions of technical facts in areas of esoteric technology must always be supported by citation to some reference work recognized as standard in the pertinent art and the appellant given, in the Patent Office, the opportunity to challenge the correctness of the assertion or the notoriety or

repute of the cited reference." (Citations omitted). *In re Pardo and Landau*, 214 USPQ 673, 677 (CCPA 1982). The support must have existed at the time the claimed invention was made. *In re Merck & Co., Inc.*, 231 USPQ 375, 379 (Fed. Cir. 1986).

"Allegations concerning specific 'knowledge' of the prior art, which might be peculiar to a particular art should also be supported and the appellant similarly given the opportunity to make a challenge." (Citations omitted). *In re Pardo and Landau*, 214 USPQ 673, 677 (CCPA 1982).

In addition, "it is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention, using the Appellant's structure as a template and selecting elements from references to fill the gaps. The references themselves must provide some teaching whereby the Appellant's combination would have been obvious." (citations omitted). *In re Gorman*, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991). *See also In re Dembiczak*, 50 USPQ2d 1614, 1616 (Fed. Cir. 1999) (reversing rejection based upon hindsight).

Moreover, the procedures established by Title 37 of the Code of Federal Regulations expressly entitle the Applicant to an Examiner's affidavit upon request. Specifically, "when a rejection in an application is based on facts within the personal knowledge of an employee of the Office, the data shall be as specific as possible, and the reference must be supported, when called for by the applicant, by the affidavit of such employee, and such affidavit shall be subject to contradiction or explanation by the affidavits of the applicant and other persons." 37 C.F.R. 1.104(d)(2). The failure to provide any objective evidence to support the challenged use of Official Notice constitutes **clear and reversible error**. *Ex parte Natale*, 11 USPQ2d 1222, 1227-1228 (Bd. Pat. App. & Int. 1989).

Despite Appellant's request in its Amendment submitted on

October 17, 2003 that the examiner supply either a reference or an Examiner's affidavit in support of the examiner's officially notice position of obviousness of what was allegedly well known, the examiner failed to provide either a reference or an affidavit. Accordingly, under M.P.E.P. § 2144.03, the assertions of what is allegedly well known must be withdrawn.

In addition, the examiner's assertion amounts to nothing more than an "obvious-to-try" situation. Specifically, "an 'obvious-to-try' situation exists when a general disclosure may pique the scientist's curiosity, such that further investigation might be done as a result of the disclosure, but the disclosure itself does not contain a sufficient teaching of how to obtain the desired result, or that the claimed result would be obtained if certain directions were pursued." *In re Eli Lilly & Co.*, 14 USPQ2d 1741, 1743 (Fed. Cir. 1990). Moreover, "an invention is 'obvious to try' where the prior art gives either no indication of which parameters are critical or no direction as to which of many possible choices is likely to be successful." *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 10 USPQ2d 1843, 1845 (Fed. Cir. 1989).

Here, Appellant's related art and Dewa do not contain a sufficient teaching of how to obtain the desired result, or that the claimed result would be obtained if certain directions were pursued. "Obvious to try" is not the standard under § 103. *In re O'Farrell*, 7 USPQ2d 1673, 1680 (Fed. Cir. 1988). Accordingly, withdrawal of the rejection of claim 43 is respectfully requested.

8. Independent Claim 44 is Not Obvious

Independent claim 44 recites a storage medium for storing in a computer-readable format routines wherein, *inter alia*, a second processing executes a next instruction after executing a

wait release instruction without suspending the second processing.

In contrast, Figure 8 of the Appellant's related art fails to disclose, teach or suggest the second processor element 114 executing a next instruction without suspending the processing of the second user program after executing the alleged wait release instruction ("end"). Instead, Figure 8 of Appellant's related art depicts the termination of the second user program after executing the alleged wait release instruction ("end"). The application of the Dewa reference additionally fails to remedy this deficiency.

Accordingly, since the applied art fails to teach each and every limitation of claim 44, a *prima facie* rejection of the claims has not been established and withdrawal thereof is respectfully requested.

## IX. CLAIMS INVOLVED IN THE APPEAL

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A represent the state of the claims as pending.

Dated: January 21, 2004

Respectfully submitted,

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**APPENDIX A- CLAIMS INVOLVED IN APPEAL**

Claims 1-22 (Cancelled).

23. (Previously presented) A parallel processor comprising, a plurality of processor elements, wherein:

a first processor element of said plurality of processor elements for executing a first user program of a plurality of user programs, said first processor element executes a wait instruction, said wait instruction suspends processing of said first user program; and

a second processor element of said plurality of processor elements for executing a second user program of said plurality of user programs, said second processor element executes a wait release instruction, said wait release instruction commands said first processor element to resume said processing of said first user program,

wherein said first processor element executes a program end instruction, said program end instruction resuming said processing of said second user program.

24. (Previously presented) A parallel processor comprising, a plurality of processor elements, wherein:

a first processor element of said plurality of processor elements for executing a first user program of a plurality of user programs, said first processor element executes a wait instruction, said wait instruction suspends processing of said first user program; and

a second processor element of said plurality of processor elements for executing a second user program of said plurality of user programs, said second processor element executes a wait release instruction, said wait release instruction commands said first processor element to resume said processing of said first user program,

wherein said second processor element executes a synchronization wait instruction, said synchronization wait instruction suspends processing of said second user program,

said wait instruction suspending processing of said first user program while resuming said processing of said second user program.

25. (Previously Presented) A parallel processor as set forth in claim 23, wherein plurality of processor elements and a common bus for connecting said plurality of processor elements are installed in a single semiconductor chip.

26. (Previously Presented) A parallel processor comprising, a plurality of processor elements, wherein:

a first processor element of said plurality of processor elements for executing a first user program of a plurality of user programs, said first processor element executes a wait instruction, said wait instruction suspends processing of said first user program; and

a second processor element of said plurality of processor elements for executing a second user program of said plurality of user programs, said second processor element executes a wait release instruction, said wait release instruction commands said first processor element to resume said processing of said first user program,

wherein said second processor element executes a next instruction without suspending said processing of said second user program after executing said wait release instruction.

27. (Previously Presented) A parallel processor as set forth in claim 23, wherein said plurality of processor elements perform mutually parallel processing on the basis of instructions written in a program and are capable of communicating with each other via a common bus.

28. (Cancelled)

29. (Previously Presented) A parallel processor as set forth in claim 23, further comprising another processor element of said plurality of processor elements for executing another user program, said another processor element executing a program end instruction, said program end instruction resuming said processing of said second user program.

30. (Previously Presented) A parallel processor as set forth in claim 23, further comprising:

a plurality of local memory, each local memory being uniquely associated with a corresponding processor element of said plurality of processor elements;

a common memory connected to a common bus, said common memory storing said plurality of user programs, a corresponding user program of said plurality of user programs being provided to said corresponding processor element via said common bus.

31. (previously presented) A parallel processor as set forth in claim 30, wherein said first processor element is said corresponding processor element and said first user program is said corresponding user program.

32. (Previously Presented) A parallel processor as set forth in claim 30, wherein said local memory continues to store said user program until said corresponding processor element executes a program end instruction indicating an end of a program.

33. (Previously Presented) A parallel processor as set forth in claim 30, wherein, when said second processor element enters a waiting state based on said wait instruction, said corresponding processor element which executed said program execution instruction executes said wait release instruction.

34. (Previously Presented) A parallel processor as set forth in claim 30, wherein:

said second processor element executes a program execution instruction, said program execution instruction commanding said corresponding processor element to receive said corresponding user program from said common memory and to execute said corresponding user program.

35. (Previously Presented) A parallel processor as set forth in claim 34, further comprising:

an arbiter for determining which of said of said plurality of processor elements executes a program instructed to be executed by said program execution instruction, and for reading the program instructed to be executed by said program execution instruction from said common memory to said local memory associated with said corresponding processor element.

36. (Previously presented) A parallel processing method comprising:

suspending processing of a first user program of a plurality of user programs, said first user program including a wait instruction, said first processor element executing said wait instruction to suspend said processing of a first user program; resuming said processing of said first user program by executing a wait release instruction, said wait release instruction being including within a second user program of a plurality of user programs, a second processor element of said plurality of processor elements for executing said wait release instruction,

said wait release instruction commanding said first processor element to resume said processing of said first user program; and

executing a program end instruction to resume said processing of said second user program, wherein said first processor element executes said program end instruction.

37. (Previously Presented) A parallel processing method as set forth in claim 36, further comprising:

suspending processing of said second user program, said second processor element executing a synchronization wait instruction.

38. (Previously presented) A parallel processing method comprising:

suspending processing of a first user program of a plurality of user programs, said first user program including a wait instruction, said first processor element executing said wait instruction to suspend said processing of a first user program; and

resuming said processing of said first user program by executing a wait release instruction, said wait release instruction being including within a second user program of a

plurality of user programs, a second processor element of said plurality of processor elements for executing said wait release instruction,

said wait release instruction commanding said first processor element to resume said processing of said first user program,

wherein in said step of suspending processing of said first user program, said processing of said first user program is suspended while resuming said processing of said second user program.

39. (Previously presented) A parallel processing method comprising:

suspending processing of a first user program of a plurality of user programs, said first user program including a wait instruction, said first processor element executing said wait instruction to suspend said processing of a first user program;

resuming said processing of said first user program by executing a wait release instruction, said wait release instruction being including within a second user program of a plurality of user programs, a second processor element of said plurality of processor elements for executing said wait release instruction,

said wait release instruction commanding said first processor element to resume said processing of said first user program; and

executing a next instruction without suspending said processing of said second user program after executing said wait release instruction, said second processor element executing said next instruction.

40. (Cancelled)

41. (Previously Presented) A parallel processing method as set forth in claim 36, wherein, when said second processor element enters a waiting state based on said wait instruction, said corresponding processor element which executed said program execution instruction executes said wait release instruction.

42. (Previously Presented) A parallel processing method as set forth in claim 36, wherein:

said second processor element executes a program execution instruction, said program execution instruction commanding said corresponding processor element to receive said corresponding user program from said common memory and to execute said corresponding user program.

43. (Previously presented) A storage medium for storing in a computer-readable format routines comprising:

first processing and second processing to be performed in parallel based on instructions written in programs, wherein

said first processing executes a wait instruction to suspend said first processing by entering said first processing into a waiting state; and

said second processing executes a wait release instruction to resume execution of said first processing,

said second processing enters a synchronization waiting state by executing said wait release instruction until said first processing enters said waiting state when said first processing is not in said waiting state.

44. (Previously Presented) A storage medium for storing in a computer-readable format routines comprising:

first processing and second processing to be performed in parallel based on instructions written in programs, wherein

said first processing executes a wait instruction to suspend said first processing; and

said second processing executes a wait release instruction to resume execution of said first processing,

said second processing executing a next instruction after executing said wait release instruction without suspending said second processing.